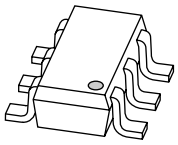


IP4234CZ6

Single USB 2.0 ESD protection to IEC 61000-4-2 level 4

Rev. 01 — 16 April 2009 Product data sheet

1. Product profile

1.1 General description

The IP4234CZ6 is designed to protect Input/Output (I/O) USB 2.0 ports, that are sensitive to capacitive loads, from being damaged by ElectroStatic Discharge (ESD). The π-filter structure is implemented with a small series resistor to provide the necessary protection to signal and supply components from ESD voltages greater than ±8 kV contact discharge according IEC 61000-4-2, level 4.

The ESD protection is independent of the supply voltage due to the rail-to-rail diode architecture being connected to a Zener diode.

The IP4234CZ6 is fabricated using monolithic silicon technology and integrates two ultra-low capacitance π-filter ESD protection diodes plus a Zener diode in a miniature 6-lead SOT457 package.

1.2 Features

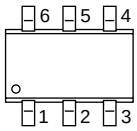
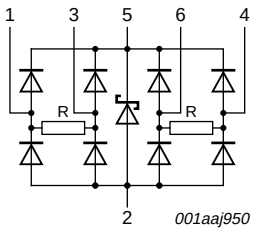
- Pb-free and RoHS compliant
- Simple, direct signal routing provides for high speed signal integrity
- ESD protection compliant to IEC 61000-4-2 level 4, ±8 kV contact discharge
- Significant reduction in peak clamping and peak residual current
- Four low input capacitance (2.0 pF typical) rail-to-rail ESD protection diodes
- Low voltage clamping due to an integrated Zener diode
- Small 6-lead SO6 (SOT457) package
- IEC 61000-4-5 15 A Lightning (8/20 μs) compliant

1.3 Applications

- General-purpose downstream ESD protection high frequency analog signals and high-speed serial data transmission for ports inside:
  - Cellular and PCS mobile handsets
  - PC/Notebook USB2.0/IEEE1394 ports
  - DVI interfaces
  - HDMI interfaces
  - Cordless telephones
  - Wireless data (WAN/LAN) systems
  - PDAs

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	ESD protection I/O channel 1		
2	ground		
3	ESD protection I/O channel 1		
4	ESD protection I/O channel 2		
5	supply voltage		
6	ESD protection I/O channel 2		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4234CZ6	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		GND – 0.5	+5.5	V
V_{esd}	electrostatic discharge voltage	all pins; IEC 61000-4-2 level 4; contact discharge	–15	+15	kV
P_{PP}	peak pulse power	t_p = 8/20 µs; IEC 61000-4-5 15 A lightning	-	100	W
T_{stg}	storage temperature		–55	+125	°C

5. Recommended operating conditions

Table 4. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		–40	+85	°C

6. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{(I/O-GND)}$	input/output to ground capacitance	pins 1, 3, 4, 6; V_I = 0 V; f = 1 MHz; V_{CC} = 3.0 V	[1]	-	2.5	-	pF
$C_{(zd-GND)}$	Zener diode to ground capacitance	pin 5 to pin 2; V_I = 0 V; f = 1 MHz; V_{CC} = 3.0 V	[1]	-	40	-	pF
I_{LR}	reverse leakage current	pins 1, 3, 4, 6 to ground; V_I = 3.0 V		-	-	100	nA
V_{BRzd}	Zener diode breakdown voltage	pin 5 to pin 2; I = 1 mA		6	-	9	V
V_F	forward voltage		[1]	-	0.7	-	V
R_s	series resistance	T_{case} = 25 °C	[1]	-	0.5	-	Ω

[1] Guaranteed by design.

7. Application information

7.1 Universal serial bus 2.0 protection

The IP4234CZ6 is optimized to protect a USB 2.0 port from ESD. The device is capable of protecting both USB data lines and the V_{BUS} supply. A typical application is shown in Figure 1.

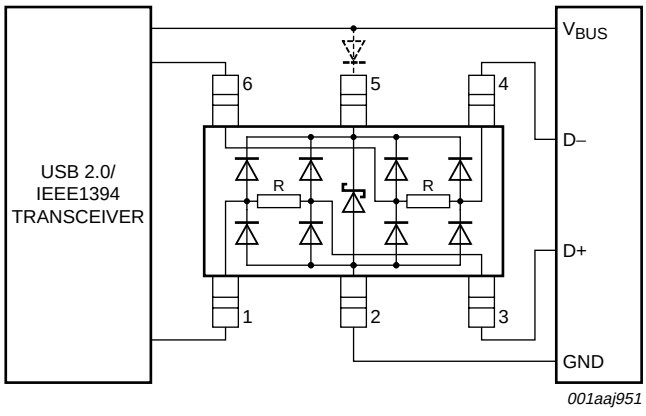
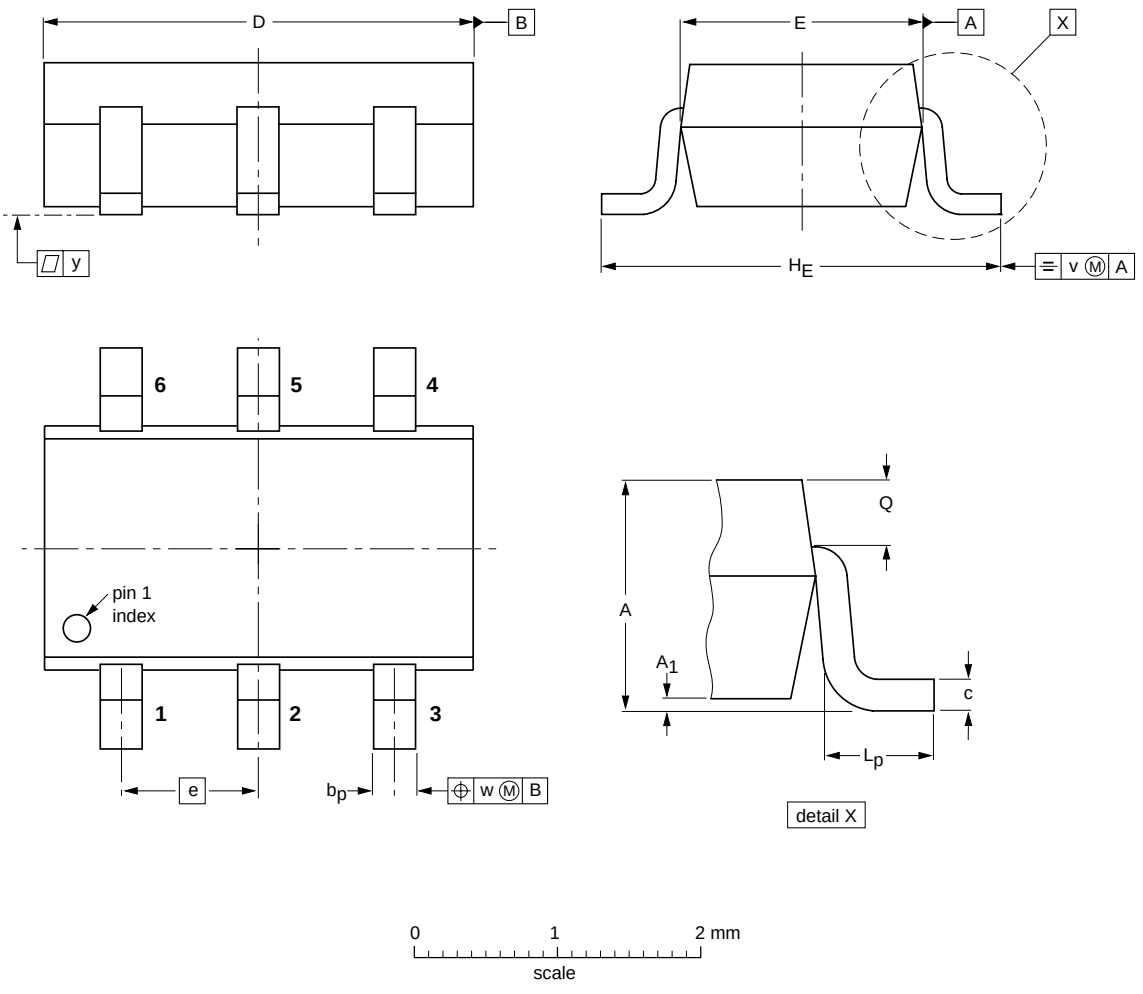


Fig 1. Typical application of IP4234CZ6

To avoid a short circuit on the data lines when V_{BUS} is shut down, a back drive protection diode can be attached to the IP4234CZ6.

8. Package outline

Plastic surface-mounted package (TSOP6); 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~05-11-07~~ 06-03-16

Fig 2. Package outline SOT457 (TSOP6)

9. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

9.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

9.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

9.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

9.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 3) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 6 and 7

Table 6. SnPb eutectic process (from J-STD-020C)

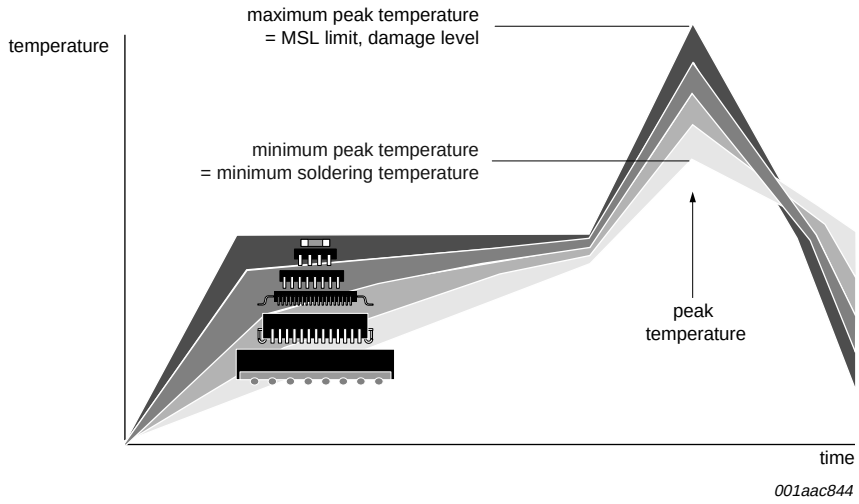
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 7. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 3.



MSL: Moisture Sensitivity Level

Fig 3. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

10. Abbreviations

Table 8. Abbreviations

Acronym	Description
DVI	Digital Video Interface
ESD	ElectroStatic Discharge
HDMI	High Definition Multimedia interface
LAN	Local Area Network
PCS	Personal Computing System
PDA	Personal Digital Assistant
RoHS	Restriction of Hazardous Substances
USB	Universal Serial Bus
WAN	Wide Area Network

11. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4234CZ6_1	20090416	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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